**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. – 2. (Cancelled)

3. (Currently Amended) The fuse detection circuit of Claim 5 ~~A fuse detection circuit, comprising:~~

~~a fust bridge circuit in which a first arm of the fuse bridge circuit has a fuse under detection, for producing a first voltage in the first arm in response to a read signal pulse;~~

~~a second arm of the fuse bridge circuit having a reference fuse, for producing a second voltage in the second arm in response to the read signal pulse, said first and second arms each having detection elements;~~

~~a sensing circuit for sensing the first voltage and the second voltage as status value data;~~

~~a latch circuit keeping the data in the sensing circuit; and~~

~~a timing control circuit to turn off the fuse bridge circuit after the latch circuit has been activated~~ wherein, the detection elements of the first arm and the second arm have different resistances.

4. (Cancelled)

5. (Previously Presented) A fuse detection circuit, comprising:

a fuse bridge circuit in which a first arm of the fuse bridge circuit has a fuse under detection, for producing a first voltage in the first arm in response to a read signal pulse;

a second arm of the fuse bridge circuit having a reference fuse, for producing a second voltage in the second arm in response to the read signal pulse;

a sensing circuit for sensing the first voltage and the second voltage as status value data;

a latch circuit keeping the data in the sensing circuit; and

a timing control circuit to turn off the fuse bridge circuit after the latch circuit has been activated, wherein, the timing control circuit has a first NAND gate receiving a first current pulse and a second current pulse as inputs, and a second NAND gate receiving an output of the first NAND gate and the read signal pulse as inputs, and an output of the second NAND gate delaying turn off of the bridge current until after the latch circuit has been activated.

6. (Original) The circuit as in Claim 5 wherein, a transition of the second current pulse turns off the timing control circuit.

7. (Original) The circuit as in Claim 5 wherein, the latch circuit extends the duration of the second current pulse relative to the duration of the read signal pulse.

8. (Previously Presented) The circuit as in Claim 3 wherein, the first arm and the second arm have respective transistors of different multiples of a gate width to gate length ratio, to adjust a burned state detection threshold for the fuse under detection.

9. (Previously Presented) The circuit as in Claim 3 wherein, the fuse under detection and the reference fuse have the same resistance prior to programming or burning the fuse under detection.

10. (Previously Presented) The circuit as in Claim 3 wherein, said different resistances are proportioned relative to one another to adjust a burned-state detection threshold for the fuse under detection.

11. – 20. (Cancelled)